CLAIMS:

1. A power amplifier comprising:

a transconductance stage that is operable to receive an input voltage signal and to produce an output current signal;

a cascode stage communicatively coupled to the transconductance stage that is operable to receive the output current signal and to produce an output voltage signal based thereupon, wherein the cascode stage includes a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar transistor formed in parallel therewith in a semi conductive substrate, wherein the MOS transistor has a drain, a gate, and a source, and wherein the corresponding parasitic bipolar junction transistor has a collector corresponding to the drain, an emitter corresponding to the source, and a base corresponding to the semi conductive substrate; and

a connector that couples the base of the corresponding parasitic bipolar junction transistor to the source of the MOS transistor.

2. The power amplifier of claim 1, wherein:

the semi conductive substrate is a P well;

the MOS transistor comprises an N type source and an N type drain formed in the P well to define a channel there between and a gate formed upon the P well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P well; and

further comprising a P+ base contact formed in the P well, wherein the connector couples the P+ base contact to the N type source.

3. The power amplifier of claim 1, wherein:

the semi conductive substrate is an N well;

the MOS transistor comprises a P type source and a P type drain formed in the N well to define a channel there between and a gate formed upon the N well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact formed in the N well, wherein the connector couples the N+ base contact to the P type source.

4. The power amplifier of claim 1, further comprising a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor.

5. The power amplifier of claim 1, wherein:

the transconductance stage comprises a transconductance element having a first terminal tied to ground and a second terminal;

the MOS transistor and the corresponding bipolar junction transistor include a shared drain/collector terminal and a shared source/emitter terminal coupled to the second terminal of the transconductance element; and

the cascode stage further comprises a circuit element coupled between a voltage supply and the shared drain/collector terminal of the MOS transistor and the corresponding bipolar junction transistor.

6. The power amplifier of claim 5, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

7. The power amplifier of claim 1, wherein:

the transconductance stage comprises:

a circuit element having a first terminal tied to a transconductance stage voltage supply and a second terminal;

a transconductance element having a first terminal coupled to the second terminal of the circuit element of the transconductance stage and a second terminal tied to ground;

the cascode stage comprises:

a first circuit element having a first terminal coupled to ground and a second terminal;

a second circuit element having a first terminal tied to a cascode stage voltage supply and a second terminal;

the source of the MOS transistor coupled to the second terminal of the first biasing element and the drain of the MOS transistor coupled to the second terminal of the second biasing element; and

the power amplifier further comprising an AC coupling stage that couples the output current signal produced by the transconductance stage to the cascode stage.

8. The power amplifier of claim 7, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

9. The power amplifier of claim 1, wherein;

the semi conductive substrate is a well formed in a semi conductive wafer; and

the connector couples between the well and the source that is formed in the well.

10. The power amplifier of claim 9, further comprising a base contact formed in the well to which the connector couples.

11. A power amplifier comprising:

a transconductance stage having a transconductance element operable to receive an input voltage signal and to produce an output current signal;

a cascode stage communicatively coupled to the transconductance stage that is operable to receive the output current signal and to produce an output voltage signal based thereupon, wherein the cascode stage includes a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar transistor formed in parallel therewith in a semi conductive substrate, wherein the MOS transistor has a drain, a gate, and a source, and wherein the corresponding parasitic bipolar junction transistor has a collector corresponding to the drain, an emitter corresponding to the source, and a base corresponding to the semi conductive substrate;

a connector that couples the base of the corresponding parasitic bipolar junction transistor to the source of the MOS transistor;

at least one circuit element; and

wherein the at least one circuit element, the transconductance element, and source and drain terminals of the MOS transistor couple in series between a voltage supply and ground.

12. The power amplifier of claim 11, wherein:

the semi conductive substrate is a P well;

the MOS transistor comprises an N type source and an N type drain formed in the P well to define a channel there between and a gate formed upon the P well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P well; and

further comprising a P+ base contact formed in the P well, wherein the connector couples the P+ base contact to the N type source.

13. The power amplifier of claim 11, wherein:

the semi conductive substrate is an N well;

the MOS transistor comprises a P type source and a P type drain formed in the N well to define a channel there between and a gate formed upon the N well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact formed in the N well, wherein the connector couples the N+ base contact to the P type source.

14. The power amplifier of claim 11, further comprising a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor.

15. The power amplifier of claim 11, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

16. The power amplifier of claim 11, wherein:

the semi conductive substrate is a well formed in a semi conductive wafer; and

the connector couples between the well and the source that is formed in the well.

17. The power amplifier of claim 16, further comprising a base contact formed in the well to which the connector couples.

18. A power amplifier comprising:

a transconductance stage having a transconductance element and at least one circuit element and operable to receive an input voltage signal and to produce an output current signal;

an AC coupling stage communicatively coupled to the transconductance stage;

a cascode stage communicatively coupled to the AC coupling stage to receive the output current signal and to produce an output voltage signal based thereupon, wherein the cascode stage includes a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar transistor formed in parallel therewith in a semi conductive substrate, wherein the MOS transistor has a drain, a gate, and a source, and wherein the corresponding parasitic bipolar junction transistor has a collector corresponding to the drain, an emitter corresponding to the source, and a base corresponding to the semi conductive substrate;

a connector that couples the base of the corresponding parasitic bipolar junction transistor to the source of the MOS transistor;

wherein the transconductance stage is biased between a transconductance stage voltage supply and ground; and

wherein the cascode stage is biased between a cascode stage voltage supply and ground.

19. The power amplifier of claim 18, wherein:

the semi conductive substrate is a P well;

the MOS transistor comprises an N type source and an N type drain formed in the P well to define a channel there between and a gate formed upon the P well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P well; and

further comprising a P+ base contact formed in the P well, wherein the connector couples the P+ base contact to the N type source.

20. The power amplifier of claim 18, wherein:

the semi conductive substrate is an N well;

the MOS transistor comprises a P type source and a P type drain formed in the N well to define a channel there between and a gate formed upon the N well above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact formed in the N well, wherein the connector couples the N+ base contact to the P type source.

21. The power amplifier of claim 18, further comprising a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor.

22. The power amplifier of claim 18, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

23. The power amplifier of claim 21, wherein the signal level detection and bias determination module is operable to turn off the MOS transistor and to controllably biases the corresponding parasitic bipolar junction transistor in an active range.

24. The power amplifier of claim 18, wherein:

the semi conductive substrate is a well formed in a semi conductive wafer; and

the connector couples between the well and the source that is formed in the well.

25. The power amplifier of claim 24, further comprising a base contact formed in the well to which the connector couples.